CLAIMS

What is claimed is:

1. A method for superword register value numbering, the method comprising:

hashing an operation code and value numbers of a plurality of sources to generate a first hash value;

retrieving an operation value number from a first hash table based on the first hash value;

generating a result value number based on a previous bit hash value and the operation value number; and

searching a second hash table using the result value number.

2. The method of claim 1 further comprising:

if the result value number is found within the second hash table, retrieving an output of the instruction from the second hash table.

3. The method of claim 1 further comprising:

if the result value number is not found within the second hash table, writing the operation value number to the second hash table.

4. The method of claim 1 further comprising:

prior to generating a result value number, retrieving the previous bit hash value.

5. The method of claim 1 further comprising:

prior to retrieving the operation value number, comparing the first hash value with a first hash table.

6. The method of claim 1 further comprising:

if the first hash value is not within the first hash table, assigning the first hash value a multiple component hash value.

7. The method of claim 1 wherein the operation value number is an n-tuple number.

8. The method of claim 1 wherein the step of generating the result value number includes:

for each component in a write mask:

if the write mask value is true, setting the result value number equal to the operation value number; and

if the write mask value is false, setting the result value number equal to a previous value number.

9. The method of claim 1 wherein the operation code and the value numbers are disposed within an instruction, the instruction further including a previous bit and a write mask.

10. An apparatus for superword register value numbering, the apparatus comprising:

at least one memory device storing a plurality of executable instructions; and

at least one processor operably coupled to the at least one memory device, operative to receive the plurality of executable instructions such that the processor, in response to the executable instructions:

hashes an operation code and value numbers of a plurality of sources to generate a first hash value;

retrieves an operation value number from a first hash table based on the first hash value;

generates a result value number based on a previous bit hash value and the operation value number; and

searches a second hash table using the result value number.

11. The apparatus of claim 10 wherein the at least one processor further in response to the executable instructions:

if the result value number is found within the second hash table, retrieves an output of the instruction from the second hash table.

12. The apparatus of claim 10 wherein the at least one processor further in response to the executable instructions:

if the result value number is not found within the second hash table, writes the operation value number to the second hash table.

13. The apparatus of claim 10 wherein the at least one processor further in response to the executable instructions:

prior to generating a result value number, retrieves the previous bit hash value.

14. The apparatus of claim 10 wherein the at least one processor further in response to the executable instructions:

prior to retrieving the operation value number, compares the first hash value with a first hash table.

15. The apparatus of claim 10 wherein the at least one processor further in response to the executable instructions:

if the first hash value is not within the first hash table, assigns the first hash value a multiple component hash value.

16. The apparatus of claim 10 wherein when the at least one processor generates the result value number, the at least one processor further in response to the executable instructions:

for each component in a write mask:

if the write mask value is true, sets the result value number equal to the operation value number; and

if the write mask value is false, sets the result value number equal to a previous value number.

17. The apparatus of claim 10 further comprising:

a superword register operably coupled to the processor, the superword register operative to store a plurality of instructions therein.

18. The apparatus of claim 10 further comprising:

at least one hash memory device operably coupled to the at least one processor such that the at least one hash memory device is operative to store the first hash table and the second hash table.

19. A method for superword register value numbering, the method comprising:

hashing an operation code and value numbers of a plurality of sources to generate a first hash value;

comparing the first hash value with a first hash table;

retrieving an operation value number from the first hash table;

retrieving the previous bit hash value;

generating a result value number based on the previous bit hash value and the operation value number;

searching a second hash table using the result value number;

if the result value number is found within the second hash table, retrieving an output of the instruction from the second hash table; and

if the result value number is not found within the second hash table, writing the operation value number to the second hash table.

20. The method of claim 19 further comprising:

if the first hash value is not within the first hash table, assigning the first hash value a multiple component hash value.

21. The method of claim 19 wherein the step of generating the result value number includes:

for each component in a write mask:

if the write mask value is true, setting the result value number equal to the operation value number; and

if the write mask value is false, setting the result value number equal to a previous value number.